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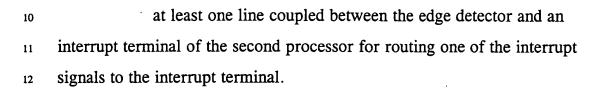
What is claimed:

- 1. In a system having first and second processors, a method
 2 of synchronizing the first processor with the second processor, comprising
 3 the steps of:
- 4 (a) storing in a register parallel bits of data from the first 5 processor, wherein at least one bit of data is a logic ONE,
- 6 (b) forming an output signal from the at least one bit of data 7 in the register, and
- 8 (c) sending the output signal to an interrupt terminal of the 9 second processor for synchronizing the first processor with the second 10 processor.
- The method of claim 1 wherein the register is a memory mapped register.
- The method of claim 1 wherein the register is an off-core register.
- 1 4. The method of claim 1 wherein at least one of the first 2 and second processors is a digital signal processor (DSP).
- 5. The method of claim 1 wherein step (b) includes
 detecting a leading edge of the at least one bit of data to form the output
 signal.



- The method of claim 5 wherein step (c) includes sending
- the output signal on a dedicated line between the register and the interrupt
- 3 terminal.
- 7. The method of claim 6 wherein the output signal is active
- 2 for a duration of a clock period.
- 1 8. The method of claim 1 including the steps of
- enabling the register during a write cycle, and
- storing the parallel bits of data when an address of the register
- 4 matches a predetermined address.
- 9. A system for providing an interrupt signal from a first
- 2 processor to a second processor comprising
- a data bus coupled to the first processor for routing parallel bits
- 4 of data,
- a register coupled to the data bus for storing the parallel bits of
- 6 data, at least one of the parallel bits of data having an active logic level,
- an edge detector coupled to the register for detecting active
- 8 logic levels stored in the register and converting each active logic level into
- 9 an interrupt signal, and





- 10. The system of claim 9 wherein the register includes a
- 2 first set of flip/flops, each flip/flop storing one of the active logic levels, and
- the edge detector includes a second set of flip/flops, each
- 4 flip/flop detecting one of the active logic levels.
- 1 The system of claim 9 further including
- an address bus coupled between the first processor and the
- 3 register, and
- a predetermined address for the register,
- wherein the first processor routes the parallel bits of data to the
- 6 register by setting the predetermined address on the address bus.
- 12. The system of claim 9 wherein the register is an off-core
- 2 register and is enabled by a write strobe signal from the first processor.
- 1 13. The system of claim 9 wherein at least one of the first
- and second processors is a DSP.



- 14. In a multi-processor system having data lines between each processor and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising
- a register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,
- a detector for detecting each of the data bits in the register, and
- a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor,
- wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.
- 15. The system of claim 14 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and
- the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.
- 16. The system of claim 14 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.
- 17. The system of claim 14 wherein at least one processor is 2 a DSP.

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- 18. The system of claim 14 further including an address bus
- 2 coupled to the register, wherein the data bits are stored in the register when
- the first processor addresses the register.
- 1 19. The system of claim 14 wherein the data bits are stored
- in the register during a first clock cycle and the data bits are detected by the
- detector during a second clock cycle, and
- the interrupt signal is enabled for a duration of a clock cycle.
- 1 20. In an integrated circuit including at least two processors,
- data lines between each processor, and at least one interrupt terminal in each
- processor, a system for synchronizing a first processor with a second
- 4 processor comprising
- a register coupled to the data lines for storing data bits from the
- 6 first processor, each data bit representing an interrupt signal,
- a detector for detecting each of the data bits in the register, and
- a signal router for routing each of the detected data bits to a
- 9 respective interrupt terminal in the second processor,
- wherein when the first processor stores a data bit in the register,
- the router provides an interrupt signal to the second processor.
- The system of claim 20 wherein the register includes a
- 2 first set of flip/flops, each flip/flop storing one of the data bits, and



- the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.
- The system of claim 20 wherein the signal router
- 2 includes a set of lines, each line connected to the respective interrupt
- 3 terminal.
- The system of claim 20 wherein at least one processor is
- a DSP.
- The system of claim 20 wherein at least one processor is
- 2 a microprocessor.
- The system of claim 20 further including an address bus
- 2 coupled to the register, wherein the data bits are stored in the register when
- 3 the first processor addresses the register.
 - 26. The system of claim 20 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.